REMARKS/ARGUMENTS

Claims 1-20 and 25 are pending. Claims 1, 3, 7, 11-13, and 19 have been amended. Claims 21-24 have been canceled. Support for the amended claims is found in the specification. No new matter has been added.

Claims 1-6, 13-18 and 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Novak et al. (6,295,586).

Claims 7-12, 19 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Novak et al. in view of Fenwick et al. (6,076,129).

Claim Rejections - 35 U.S.C. § 102(e)

Claim 1 has been amended to recite "a queue comprising a plurality of request stations, wherein each of the plurality of memory transactions is stored in one of the request stations and is addressed to one of the plurality of memory banks; and an arbiter simultaneously coupled to each of the plurality of request stations" and "adapted to select any of the plurality of memory transactions" among other claim elements. The Applicants respectfully submit that at least these claim elements are not taught or suggested by the cited reference.

As described in the specification, a queue includes a plurality of request stations 112A through 112N, each request station storing a memory transaction destined for one of a plurality of memory banks. As illustrated in figure 2, the arbiter is simultaneously coupled to each of the plurality of request stations and generates bank readiness signals BNKRDYA through BNKRDYM. The arbiter is adapted to select any of the plurality of memory transactions from the queue based on the readiness of the memory banks to accept a memory transaction. (Specification at page 4, lines 19-30 and Figure 2). Because the arbiter is able to select any of the plurality of memory transactions from the queue, the selection of a memory transaction is not limited the memory transaction stored in the final request station, for example, request station 112N in figure 2. (See Specification at page 11, lines 13-25 and figure 7).

In contrast, Novak appears to discuss several queues (AQ, PQ, and RWQ) that are independently connected to the multiplexer SPM 370. (Novak at col. 8, line 66 to col. 9, line 5 and figure 2). As illustrated in figure 2 of Novak, only the bottom entry of each queue is connected to the multiplexer SPM. Taking the RWQ as an example, only the bottom entry of the

RWQ is connected to the SPM. Thus, the SPM is only able to select a subset of the queue entries (the bottom entries).

Therefore, in contrast with the present invention, Novak fails to teach or suggest "an arbiter simultaneously coupled to each of the plurality of request stations" and "adapted to select any of the plurality of memory transactions," as recited by claim 1. For at least these reasons, claim 1 is in a condition for allowance.

Claims 2-6, which depend from claim 1, are in a condition for allowance, for at least the reasons discussed in relation to claim 1, as well as for the additional limitations they recite.

Claim 13 recites "means for generating a first bank readiness signal by monitoring an address of a first one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the first bank readiness signal indicates the readiness of one of the memory banks to accept the first one of the plurality of memory transactions; means for generating a second bank readiness signal by monitoring an address of a second one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the second bank readiness signal indicates the readiness of another of the memory banks to accept the second one of the plurality of memory transactions; and means for selecting a third one of the memory transactions for transmission over the memory bus based on at least one of the first bank readiness or the second bank readiness signal" among other claim elements. The Applicants respectfully submit that at least these claim elements are not taught or suggested by the cited reference.

As illustrated in figure 2 of the specification, in one embodiment, the state machine 204 "monitors the addresses of the memory transactions that are gated to memory 104" over memory bus 106 at a location along the memory bus. (Specification at page 5, lines 14-15). "In particular, state machine 204 monitors each memory transaction gated across memory bus 106 to determine which memory bank 116 will receive that memory transaction." "After a predetermined period of time has elapsed, state machine 204 sets the bank readiness signal for that memory bank 116, thereby indicating that that memory bank 116 is available to accept another memory transaction." (Specification at page 5, lines 18-25). Thus, the arbiter is able to

select a subsequent memory transaction based on monitoring of previous memory transactions gated across the memory bus.

Novak, on the other hand, discusses a memory controller in which "[e]ach of the operation queues 340, 350, 360 are operation requesters." The operation queues "assert a signal to the SPM" that "tells the SPM 370 that there is an operation ready to be sent." (Novak at col. 11, lines 11-15, emphasis added). Thus, Novak appears to disclose a memory controller with operation queues AQ, PQ and RWQ operative to generate ready signals. However, as illustrated in figure 2 of Novak, these operation queues do not monitor the addresses of memory transactions gated across the memory bus at a location along the memory bus. On the contrary, the operation queues are located upstream of the SPM and are not operable to monitor the addresses of memory transactions at a location along the memory bus, downstream of the multiplexer. Because at least these claim elements are not taught or suggested by the prior art, claim 7 is in a condition for allowance.

Claims 14-18 and 20, which depend from claim 13, are in a condition for allowance, for at least the reasons discussed in relation to claim 13, as well as for the additional limitations they recite.

Claim Rejections - 35 U.S.C. § 103(a)

Claim 7 recites "generating a first bank readiness signal by monitoring an address of a first one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the first bank readiness signal indicates the readiness of one of the memory banks to accept the first one of the plurality of memory transactions; generating a second bank readiness signal by monitoring an address of a second one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the second bank readiness signal indicates the readiness of another of the memory banks to accept the second one of the plurality of memory transactions; and selecting a third one of the memory transactions for transmission over the memory bus based on at least one of the first bank readiness or the second bank readiness signal" among other claim elements. The Applicants respectfully submit that neither the cited references, either taken alone or in combination, teach or suggest at least these claim elements.

As discussed in relation to claim 13, Novak discusses a memory controller in which each of the operation queues are operation requesters and does not teach or suggest monitoring memory transactions downstream of the multiplexer. Fenwick appears to provide a mechanism in which the "processor, memory, and I/O node monitors the data bus 46 SEND_DATA line to keep track of the number of data transactions that have occurred in order to determine when it should become a data bus commander." (Fenwick at col. 18, lines 50-54, emphasis added). However, Fenwick does not teach or suggest monitoring individual memory transactions and then selecting a subsequent memory transaction based on the process of monitoring the previous memory transactions gated across the memory bus. Fenwick merely discusses monitoring a total number of data transactions that have occurred. For at least these reasons, claim 7 is in a condition for allowance.

Claims 8-12, which depend from claim 7, are in a condition for allowance, for at least the reasons discussed in relation to claim 7, as well as for the additional limitations they recite.

Claim 19 recites a "computer program product" "operable to cause a programmable processor to: identify a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks and stored in a request station provided in a queue; generate a plurality of bank readiness signals based upon a content of the memory bus by monitoring the addresses of a first group of the plurality of memory transactions gated across the memory bus at a location along the memory bus, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and select an additional one of the plurality of memory transactions for transmission over the memory bus based on the bank readiness signals" among other claim elements. The Applicants respectfully submit that neither the cited references, either taken alone or in combination, teach or suggest at least these claim elements.

As discussed in relation to claim 7, Novak does not teach or suggest monitoring memory transactions downstream of the multiplexer. Fenwick merely discusses monitoring a total number of data transactions, not monitoring individual memory transactions and then selecting a subsequent memory transaction based on this monitoring process. For at least these reasons, claim 7 is in a condition for allowance.

Claim 25, which depends from claim 19, is in a condition for allowance, for at least the reasons discussed in relation to claim 19, as well as for the additional limitations it recites.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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